P-166: Successive Cross Emission Driving for 3-Dimensional Active-Matrix Organic Light Emitting Diode Displays

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Abstract
We propose a pixel structure and its driving scheme for stereoscopic 3-dimensional (3D) active-matrix organic light emitting diode (AMOLED) displays. The proposed pixel structure and its driving scheme have merits that are longer emission and programming time than simultaneous emission scheme by successive cross emission of left and right images. Moreover, it can reduce flicker by reducing interval between emission times. For 3D AMOLED displays of 40-inch full high definition TV (1920×1080), the emission current error rate of the proposed pixel structure is from -0.961% to 1.013% when the threshold voltage variation of driving TFT varies from -0.8 V to 0.8 V, and that the error is less than 2% when the $V_{DD}$-IR drop voltage becomes 2.0 V.

1. Introduction
Active-matrix organic light emitting diode (AMOLED) displays have several good properties such as fast response time, wide viewing angle, and excellent color reproducibility [1, 2]. Especially, the fast response time is a suitable property for stereoscopic 3-dimensional (3D) displays because it is very important to separate image frames for left and right eyes without superposition by fast response time. If the adjacent frame images for left and right eyes are superposed each other, the left-right (L-R) crosstalk occurs [3, 5]. To solve this problem, most of shutter glass type stereoscopic 3D driving schemes use methods that the frame rate is increased up to 240Hz [4] or the additional black image is inserted between adjacent frame images at 120Hz frame rate [5].

Simultaneous emission scheme is more effective than progressive emission scheme by efficient vertical blanking insertion for preventing L-R crosstalk [5]. However, simultaneous emission scheme has a limitation that the line time and the emission time are reduced for realizing high frame rate and high resolution because of time diminution assigned to one scan line. Moreover, the emission current has to be increased as much as decreased emission time, and the flicker can occur easily owing to long interval between emission phases.

We propose a pixel structure and driving scheme for stereoscopic 3D AMOLED displays that both programming time and emission time can be increased by crossing successfully emission and program phase of each frame for left or right eye. By the proposed method, we can obtain long emission and programming time, low OLED emission current, and reduction of flicker.

2. Proposed driving scheme
Figure 1 shows simultaneous emission driving scheme [5]. The scheme is that the frame for left eye (left frame) is emitted after programming data for left frame during 1/2 frame, and the frame for right eye (right frame) is emitted after programming data for right frame during the rest 1/2 frame. If the 3D AMOLED displays are driven by using this scheme, the each emission time of left and right frame is limited to less than 1/2 frame time except programming time. It means that the luminance and OLED current during emission time have to be increased. Furthermore, if emission time is increased, programming time or compensation time should be reduced as much as increased emission time. Therefore, the simultaneous emission driving scheme is difficult to obtain enough time to program data or emit OLED. If high resolution or high frame rate display is required, various problems such as lack of data programming time, insufficient compensation time, and drastic decline of luminance would be occurred. Furthermore, the flicker can be seen because the interval of emission phase for left or right frame is more than minimum 1/2 frame.

Figure 2 shows proposed successive cross emission driving scheme. The scheme is that left frame is emitted during programming time of right frame, and the right frame is emitted during programming time of left frame. In other words, the pixel for one side frame is emitted without wasted time while pixel for the other side frame is programmed by successive cross emission driving. Therefore, the proposed scheme can be more increased emission time or programming time than conventional emission schemes, and the program capability can be enhanced by increased programming time or compensation time of current error factors such as threshold voltage variation or $V_{DD}$-IR drop. Moreover, we can reduce the emission current at left or right frame during 1-frame time due to increased emission time. In addition, flicker problem is occurred due to long interval time between emission of left and right frame at conventional stereoscopic 3D driving, but we can easily reduce flicker by the proposed scheme because of relatively short interval between emission periods of each frame.

For L-R crosstalk free, we insert non-emission period that block out emission light by external shutter such as glasses during left/right conversion time between left and right emission phases. If the response speed of shutter is high, the loss of luminance can be minimized.
3. Proposed pixel structure

Figure 3 and 4 show the proposed pixel structure and timing diagram, respectively. The proposed pixel structure consists of eight p-type switching TFTs (P1, P2, P5-P10), two p-type driving TFTs (P3, P4), two storage capacitors (C1, C2), four horizontal control lines (SCAN1, SCAN2, EM1, EM2) and one additional power line (V_SUS). The operation of right side is symmetrical as that of left side. So, we explain about only left side in below driving sequence.

1) Initializing phase: The function in this phase is resetting the gate node of driving TFT. All switching TFTs controlled by SCAN1 and EM1 signals are turned on as SCAN1 and EM1 are low. Then voltage of gate node of P3 becomes initializing as low voltage. On the other hand, all switching TFTs controlled by SCAN2 and EM2 signals are turned off as SCAN2 and EM2 are high. Then C2 is floating, and the charge stored at C2 is kept by next emission phase.

2) Program phase: The purpose of next phase is programming the data voltage and compensating the threshold voltage variation of driving TFT. During this phase, EM1 goes to high, and P1 and P9 are turned off. While SCAN1 goes to low, P5 and P7 still turn on, and then the left frame data voltage \( V_{\text{DATA, left}} \) is programmed through P7. Therefore the voltage of node A changes to \( V_{\text{DATA, left}} \), and that of node B changes to \( V_{\text{DD}} - V_{\text{TH, P3}} \) by diode connection. On the other hand, EM2 goes to low, and P2 and P10 is turned on. Therefore, right frame is emitted by programmed right data during previous program phase.

3) Emission phase: SCAN1 goes to high and EM1 goes to low. Then both P5 and P7 are turned off, and both P1 and P9 are turned on. At that time, the voltage of node A changes from \( V_{\text{DATA, left}} \) to \( V_{\text{SUS}} \), \( V_{\text{DATA, left}} + V_{\text{DD}} - V_{\text{TH, P3}} \). The C1 continues to sustain the voltage for \( V_{\text{DATA, left}} - V_{\text{DD}} + V_{\text{TH, P3}} \) and this voltage holds until the next initial phase. Finally, OLED on left frame is emitted with compensation of threshold voltage variation and \( V_{\text{DD}} \)-IR drop, and the drain current of the P3 \( (I_{\text{OLED}}) \) can be written as follows:

\[
I_{\text{OLED}} = \frac{k}{2} (V_{G_{\text{S, P3}}} - V_{\text{TH, P3}})^2
= \frac{k}{2} (V_{\text{DD}} - (V_{\text{DD}} - V_{\text{TH, P3}}) - V_{\text{TH, P3}})^2
= \frac{k}{2} (V_{\text{DATA, left}} - V_{\text{DD}})^2
\]

(1)

where \( k, V_{G_{\text{S, P3}}}, \) and \( V_{\text{TH, P3}} \) are \( \mu_pC_{\text{Ox}}W/L \), the gate-source voltage of P3, and the threshold voltage of P3, respectively. \( \mu_p, C_{\text{Ox}}, W \) and \( L \) is mobility of transistor, capacitance of gate oxide, width and length of transistor, respectively.

On the other hand, P6 and P8 turn on while SCAN2 goes to low. The right frame data voltage \( (V_{\text{DATA, right}}) \) is programmed through P8.
4. Simulation Results

We verify the performance of the proposed pixel structure and driving scheme by HSPICE simulation using RPI poly-Si TFT model. Table I shows detailed simulation conditions.

Figure 5(a) shows the simulated waveform in regard to threshold voltage variation of driving TFT. The OLED current error rate of the proposed pixel structure is from -0.961% to 1.013% when the threshold voltage variation of driving TFT varies from -0.8 V to 0.8 V. Detailed simulation results for several conditions of threshold voltage variation are shown by Figure 5(b).

Figure 6(a) shows the simulated waveform in regard to VDD-IR drop and Figure 6(b) shows OLED current error rate by VDD-IR drop. When the VDD-IR drop voltage in the same pixel is 2.0 V, the OLED emission current error rate is less than 2% at maximum current level.

In conclusion, those simulation results show that emission and program in the proposed pixel structure occur in rotation per each frame as expected and the threshold voltage variation and VDD-IR drop in the pixel are properly compensated.

### Table I. Simulation conditions.

<table>
<thead>
<tr>
<th>Design parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_DD (V)</td>
<td>14</td>
</tr>
<tr>
<td>V_SS (V)</td>
<td>0</td>
</tr>
<tr>
<td>V_SUS (V)</td>
<td>2</td>
</tr>
<tr>
<td>(W/L)Switching TFT (μm)</td>
<td>5 / 7</td>
</tr>
<tr>
<td>(W/L)Driving TFT (μm)</td>
<td>5 / 20</td>
</tr>
<tr>
<td>Storage capacitor (pF)</td>
<td>1</td>
</tr>
<tr>
<td>Max. emission current (μA)</td>
<td>12</td>
</tr>
<tr>
<td>Target application</td>
<td>40-inch Full HD TV</td>
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</tbody>
</table>
5. Conclusion

We proposed the new pixel structure and its driving scheme adopted successive cross emission concept for stereoscopic 3D AMOLED displays. The programming and emission time can be increased by using the proposed driving scheme compared with simultaneous emission scheme. Therefore, we can reduce the emission current of OLED during emission phase as much as increased emission time. If we would increase the programming time, we can secure enough time for program and compensation under relatively short scan line time. In addition, flicker problem can easily resolved due to short interval time between emission phases of left and right frame. When the threshold voltage variation of driving TFT is from -0.8 V to +0.8 V, the error rate of OLED emission current is from -0.961% to 1.013%, and that is less than 2% till the V_{DD}-IR drop voltage becomes 2.0 V. Therefore, the proposed pixel structure and driving scheme can be used usefully for high resolution large-size stereoscopic 3D AMOLED displays.

6. References


